CLAIMS

1. A method of fabricating an integrated circuit having a reduced threshold voltage shift in a semiconductor substrate, comprising the steps of:

(a) forming a nonconducting region upon said semiconductor substrate;

(b) forming active regions upon said semiconductor substrate wherein said active regions are separated by said nonconducting region;

(c) depositing a barrier layer over said nonconducting region and over said active regions;

(d) depositing a dielectric layer formed from an organic precursor; and

(e) heating said barrier layer and said dielectric layer to a temperature of at least 550° C.

2. The fabrication method of claim 1, wherein said barrier layer has a thickness of between approximately 50 angstroms and approximately 2,000 angstroms.

3. The fabrication method of claim 2, wherein said barrier layer has a thickness of between approximately 100 angstroms and approximately 1,000 angstroms.

4. The fabrication method of claim 1, wherein said active regions comprise transistor elements.

5. The fabrication method of claim 1, wherein said nonconducting region comprises a field oxide region.

6. The fabrication method of claim 1, wherein said nonconducting region comprises a trench between two active regions.

7. The fabrication method of claim 1, wherein said active regions are located within an n-well.

8. The fabrication method of claim 7, wherein a plurality of integrated circuit transistors is formed within said n-well.

9. The fabrication method of claim 1, wherein said active regions are located within a p-well.

10. The fabrication method of claim 9, wherein a plurality of integrated circuit transistors is formed within said p-well.

11. The fabrication method of claim 1, wherein said active regions are diffusion regions.

12. The fabrication method of claim 11, wherein a plurality of integrated circuit transistors is formed within said diffusion regions.

13. The fabrication method of claim 1, wherein said dielectric layer comprises a BPSG layer formed from an organic precursor.

14. The fabrication method of claim 1, wherein said dielectric layer comprises a BSG layer formed from an organic precursor.

15. The fabrication method of claim 1, wherein said dielectric layer comprises a PSG layer formed from an organic precursor.

16. The fabrication method of claim 13, comprising the further step of reacting a material selected from the group consisting of TEOS, TEPO and TEB to form said BPSG.

17. The fabrication method of claim 1, wherein said barrier layer comprises silane oxide.

18. The fabrication method of claim 1, wherein said barrier layer comprises silane oxynitride.

19. The fabrication method of claim 1, wherein said barrier layer comprises a nitride film.

20. The fabrication method of claim 1, wherein said barrier layer comprises a plasma nitride film.

21. The fabrication method of claim 1, wherein said barrier layer comprises silane nitride.

22. The fabrication method of claim 1, wherein said barrier layer comprises nitride with silane oxide deposited thereupon.

23. The fabrication method of claim 1, wherein said barrier layer comprises a composite film formed of silicon dioxide and silicon nitride layers.

24. The fabrication method of claim 1, wherein said barrier layer comprises layers of oxide with a nitride film therebetween.

25. The fabrication method of claim 13, comprising a further barrier layer deposited over said BPSG layer and a further BPSG layer deposited over said further barrier layer.

26. The fabrication method of claim 1, comprising the step of performing rapid thermal processing of said layers.

27. The fabrication method of claim 26, comprising the step of heating said barrier and dielectric layers to approximately between 850°C and 1050°C for at least five seconds.

28. The fabrication method of claim 1, comprising the step of heating said barrier and dielectric layers in a furnace to between approximately 750°C and approximately 1000°C for at least five minutes.

29. The fabrication method of claim 1, comprising the step of applying a plasma treatment to said semiconductor surface prior to performing step (c) and step (d).

30. The fabrication method of claim 29, comprising the step of applying a plasma selected from the group consisting of oxygen plasma, ozone plasma, nitrogen plasma and ammonia plasma.

31. The fabrication method of claim 30, comprising the step of applying a plurality of said plasmas of said group.

32. The fabrication method of claim 1, wherein said dielectric layer has a thickness greater than one thousand angstroms.

33. The fabrication method of claim 1, wherein said barrier layer comprises oxynitride having a refractive index between approximately 1.46 and 2.0.

34. The fabrication method of claim 1, wherein said barrier layer comprises silicon rich oxynitride having a refractive index between approximately 2.0 and 2.6.

35. The fabrication method of claim 29, further comprising the step of depositing a dielectric layer directly upon said plasma treated surface.

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